WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising a RAM macro, including:

memory arrays divided into four memory arrays in the X and Y coordinates directions;

a first input circuit provided at the center of said four memory arrays for receiving a first signal; and

a second input circuit provided between two memory arrays which are disposed side by side in the direction of said Y coordinate among four memory arrays for receiving a second signal,

wherein a signal line for transferring said first and second signals to said first and second input circuits from the external side of said RAM macro is formed using an upper layer wiring for the wiring to form said memory array, and

wherein said upper layer wiring is formed in the area to form a system wiring for connecting macros.

2. A semiconductor integrated circuit device according to claim 1, further comprising a data output circuit provided at the end part in the direction of Y coordinate.

3. A semiconductor integrated circuit device according to claim 1 or 2, wherein said first signal includes a clock signal and a clock enable signal and

said second signal includes a data signal.

4. A semiconductor integrated circuit device according to claim 1,

wherein each memory array divided at the center of Y coordinate where said second input circuit is provided includes a column switch and a sense amplifier, and

wherein an output line of said sense amplifier is connected to a data output circuit .

5. A semiconductor integrated circuit device according to claim 4, wherein a sense output of low amplitude is transferred to the output line of said sense amplifier.

6. A semiconductor integrated circuit device according to claim 3, further comprising a circuit corresponding to an input/output signal for test.

7. A semiconductor integrated circuit device according to claim 2, wherein any one of end parts of said RAM macro is provided adjacently to the end part of a semiconductor chip, except for the end part, where said data output circuit is provided, among four end parts forming said RAM macro.

8. A semiconductor integrated circuit device according to claim 1, further comprising an input/output circuit for test.

9. A semiconductor integrated circuit device according to claim 8, further comprising a test pattern

generating circuit for generating a test pattern and an expectancy value thereof to be supplied to said RAM macro,

wherein said input/output circuit for test includes a switch circuit for switching the input of test pattern and input of ordinary operation and a comparing and judging circuit for comparing an output signal read from said RAM macro with said expectancy value.

10. A semiconductor integrated circuit device according to claim 9,

wherein said RAM macro is formed of a plurality of macros, and

wherein said test circuit is further provided with a RAM macro selection circuit for designating test object RAM macros among a plurality of RAM macros to conduct the test operation to the RAM macros selected with said RAM macro selection circuit.

11. A semiconductor integrated circuit device, comprising a RAM macro, including:

a first region, a second region and a third region which are respectively formed in the square shape and are disposed continuously in this sequence in the first direction;

a fourth region, a fifth region and a sixth region which are respectively formed in the square shape and are disposed continuously in this sequence in said first

direction; and

a seventh region, an eighth region and a ninth region which are respectively formed in the square shape and are disposed continuously in this sequence in said first direction,

wherein said first, fourth and seventh regions are continuously disposed in this sequence in the second direction which is perpendicular to said first direction,

wherein said second, fifth and eighth regions are continuously disposed in this sequence in said second direction,

wherein said third, sixth and ninth regions are continuously disposed in this sequence in said second direction,

wherein a first memory array including a plurality of first memory cells is formed to said first region,

wherein a second memory array including a plurality of second memory cells is formed to said third region,

wherein a third memory array including a plurality of third memory cells is formed to said seventh region,

wherein a fourth memory array including a plurality of fourth memory cells is formed to said ninth region, and

wherein an input terminal of said RAM macro is disposed to at least one region among said fourth, fifth

and sixth regions.

12. A semiconductor integrated circuit device according to claim 11,

wherein said input terminal of RAM macro is connected to a signal line formed on the predetermined wiring layer and is extended for disposition from an external side of said RAM macro, and

wherein said signal line is not defined with said RAM macro.

13. A semiconductor integrated circuit device according to claims 11 and 12, wherein said signal line is defined with an automatic disposition wiring in the chip side.

14. A semiconductor integrated circuit device according to claim 11, wherein a word line driver is disposed in said second and eighth regions.

15. A semiconductor integrated circuit device according to claim 11, wherein each of said second, fourth, fifth, six and eighth regions is smaller than each of said first, third, seventh and ninth regions.

16. A semiconductor integrated circuit device according to claim 15, wherein said fifth region is disposed to the center of said RAM macro.

17. A semiconductor integrated circuit device, including:

a first region, a second region and a third region which are respectively formed in the square shape and

continuously disposed in the first direction;

a fourth region, a fifth region and a six region which are respectively formed in the square shape and continuously disposed in said first direction; and

a seventh region, an eighth region and a ninth region which are respectively formed in the square shape and continuously disposed in said first direction;

wherein said first, fourth and seventh regions are continuously disposed in this sequence in the second direction which is perpendicular to said first direction,

wherein said second, fifth and eighth regions are disposed continuously in this sequence in said second direction,

wherein said third, sixth and ninth regions are disposed continuously in this sequence in said second direction,

wherein a first memory array including a plurality of first memory cells is formed in said first region,

wherein a second memory array including a plurality of second memory cells is formed in said third region,

wherein a third memory array including a plurality of third memory cells is formed in said seventh region,

wherein a fourth memory array including a plurality of fouroth memory cells is formed in said ninth region,

wherein each of said second, fourth, fifth, sixth and eighth regions is smaller than each of said first, third, seventh and ninth regions, and

wherein at least a part of the address input circuit is formed in said fifth region.

18. A semiconductor integrated circuit device according to claim 17, wherein a clock signal generating circuit is further disposed in said fifth region.

19. A semiconductor integrated circuit device according to claim 17, wherein a word line driver is disposed in said second and eighth regions.

20. A semiconductor integrated circuit device according to claim 17, wherein a tenth region in contact with said first, second and third regions is further included, and a data output circuit is formed in said tenth region.

21. A semiconductor integrated circuit device according to claim 20, wherein said tenth region is an end part of said RAM macro.

22. A semiconductor integrated circuit device, including:

a first region, a second region and a third region which are formed in the square shape and disposed continuously in the first direction;

a fourth region, a fifth region and a sixth region which are formed in the square shape and disposed continuously in said first direction; and

a seventh region, an eighth region and a ninth region which are formed in the square shape and disposed continuously in said first direction,

wherein said first, fourth and seventh regions are continuously disposed in this sequence in the second direction which is perpendicular to said first direction,

wherein said second, fifth and eighth regions are continuously disposed in this sequence in said second direction,

wherein said third, sixth and ninth regions are continuously disposed in this sequence in said second direction,

wherein a first memory array including a plurality of first memory cells is formed in said first region,

wherein a second memory array including a plurality of second memory cells is formed in said third region,

wherein a third memory array including a plurality of third memory cells is formed in said seventh region,

wherein a fourth memory array including a plurality of fourth memory cells is formed in said ninth region,

wherein each of said second, fourth, fifth, sixth and eighth regions is smaller than each of said first, third, seventh and ninth regions, and

wherein at least a part of the clock input circuit

is formed in said fifth region.

23. A semiconductor integrated circuit device according to claim 22, wherein a clock enable signal input circuit is further disposed in said fifth region.

24. A semiconductor integrated circuit device according to claim 22, wherein a word driver is disposed in said second and eighth regions.

25. A semiconductor integrated circuit device according to claim 22, wherein the tenth region which is in contact with said first, second and third regions is further included and the data output circuit is formed in said tenth region.

26. A semiconductor integrated circuit device according to claim 25, wherein said tenth region is the end part of said RAM macro.